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Reliability-Performance Trade-offs in Photonic NoC Architectures

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Reliability-Performance Trade-offs in Photonic NoC Architectures

By

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Dedication

Dedicated to my parents Mrs. Kanagalakshmi Thiyagarajan

And Dr. Kaliraj Subba Naicker.

Acknowledgements

I would like to express my great appreciation to my primary advisor Dr. Amlan Ganguly for his constant guidance, patience and support that he extended throughout the duration of this work. Dr Ganguly was always there to review my work and give valuable suggestions which always helped in keeping the work right on track.

Also, I would also like to thank my parents, Sister Supriya Kaliraj and friends for their encouragement and heartfelt support during the course of this work.

Abstract

Advancements in the field of chip fabrication has facilitated in integrating more number of transistors in a given area which lead to the era of multi-core processors. Interconnect became the bottleneck for the multi-core processors as the number of cores in a chip increased. The traditional bus based architectures, which are currently used in the processors, cannot scale up to support the increasing number of cores in a multi-core chip. Hence, Network-on-Chip (NoC) is the preferred communication backbone for modern multicore chips. However, the multi-hop data transmission using wireline interconnects result in high energy dissipation and latency. Hence, many alternative interconnect technologies have been proposed such as 3D, wireless, and photonic interconnects. These interconnect technologies have their own advantages and disadvantages.

Photonic interconnects have emerged as a promising alternative to the conventional metal/dielectric based on-chip wireline interconnects. Several novel architectures have been proposed using photonic waveguides as interconnects, which are capable of reducing the energy dissipation in data transfer significantly. However, the issues of reliability arising due to waveguide losses and adjacent channel crosstalk in photonic waveguides have not received much attention till date. In this paper we propose and evaluate the performance of a photonic NoC architecture designed by segmenting the waveguides into smaller parts to limit the waveguide losses and signal degradation from electro-optic devices. Through detailed system level simulations in this work we compare the performance of the

MSB-PNoC with other PNoC architectures proposed in the recent literature and establish its gains over completely electronic mesh based counterparts.

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Chapter 1 Introduction

The increase in computational complexities and ever growing databases demand more powerful computers. The fields such as astrophysics, quantum mechanics, weather research, oil and gas exploration to name a few demands more computation power from the computers. In order to satiate the hunger for computational power; lot of research has been put into making better computers. The processors that run these computers are made better every day. Number of transistors that are fabricated on a given area in a chip is increasing in accordance with the Moore's law and with clock speed not getting any faster, multi-core chips have the potential to be the driving force of the future computers. Multi-core chips of future require better performance and reliability from interconnects, which the present interconnect technologies cannot support.

1.1 Era of Multi-core processors

Performance of the processors was improved by increasing the clock speeds in the past. The requirements of the computers have increased such that increasing just the clock speed will not be possible anymore. The clock speed was increased by increasing the depth of pipelines. Deeper pipeline are no longer profitable as the flip-flops delay is comparable to the combinational logic delay. Also, the higher clock speeds mean increase in power requirements, as the power consumed by the processor is proportional to the clock frequency. Hence processors running at high frequencies are not suitable for low power devices. With the option of increasing the frequency to improve the performance getting difficult, multi-core chips is the

future of computing [1]. Deep submicron fabrication technologies enable us to pack more number of transistors. This opportunity can be used to fabricate chips with multiple numbers of cores in them. Multi-core chips are faster with parallel processing capabilities and provide high energy efficiency. With multiple cores parallel working on a problem, the multi-core chips are faster than uni-core processors for a given clock frequency under ideal conditions. Multiple cores on the chip can be controlled independently. Some of the cores can be turned off for tasks that require lesser computational power. This make the multi-core chips the ideal for low power devices.

With multi-core chips, better interconnect are required to tap their full potential. The multi-core chips use multiple cores within it to execute a large task. Hence the cores should communicate frequently between themselves with lesser latency and energy. Traditional planar dielectric interconnects cannot deliver the requirements of multi-core chips. Interconnects determine the system performance as the number of cores increases in a multi-core chips. Hence new interconnect options are studied to support the increasing number of cores in a multi-core Chip.

1.2 Interconnects in Multi-Core chips

Initially, multi-core chips used shared memory to communicate between them. As the number of cores increased, need for more sophisticated interconnects rose. Bus based, crossbar based, packet based interconnect architectures were developed. Bus based interconnect architectures are used by Intel and AMD. Quickpath interconnect from Intel is a point-to-point interconnect. It uses 20 bit

wide bus running at 3.2 GHz to communicate between cores [2]. AMD's Hyper Transport 3.0 is a 32-bit wide bus running at 5.2 GHz [3].

1.3 Network on Chip paradigm

The scalability can be achieved by having a modular interconnection network. The modular design is achieved by using on-chip interconnection networks. This approach separates the cores from communication networks. This paradigm is called as Network on Chip (NoC) [4]. Data are converted into packets and they are routed across the networks through switches. The network logic replaces the global wires, making the interconnect architecture better in terms of performance and scalability. Fig. 1-1 shows the NoC architecture.

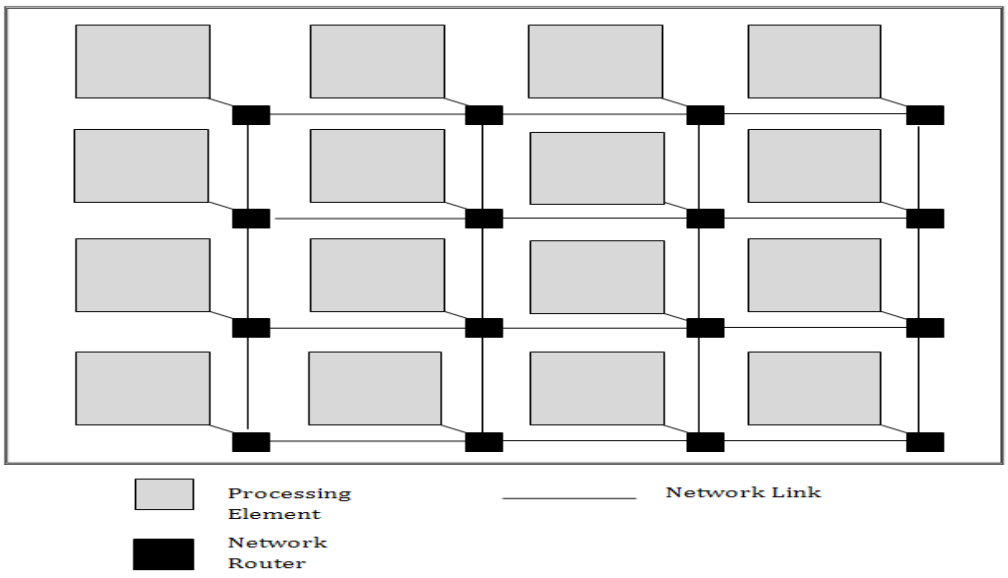

Figure 1-1 Network-on-Chip architecture

The data from the source will be delivered at the destination through either one of the following switching techniques; Circuit Switching, Packet switching, and Wormhole switching. In circuit switching, dedicated links are established between

the source and destination. Other nodes have to wait until the data transmission is finished to use the link. Hence, circuit switching cannot be used in networks with high traffic. The packet is decimated into packets and the individual packets are transmitted across the network independently through switches. The packets will be rearranged at the destination. The packet switching technique places a huge overhead on the switches in network. Each packet has to be processed at the switches. The packets should be stored in buffers at the switch if the switches are busy processing other packets. The increase in buffer size of the switches will increase the total area of the NoC architecture.

In Worm hole routing, the packets is divided into smaller units called flits. The size of the flit is determined such that, each flit can be transmitted in a single cycle. The header flit contains the routing information. The header flit will traverse across the network and setup the path for rest of the body flits. The path setup by the header flit blocks the other communications. The virtual channels are introduced in order to alleviate this problem. The switches have buffers to store the flits until a path is available to transmit them.

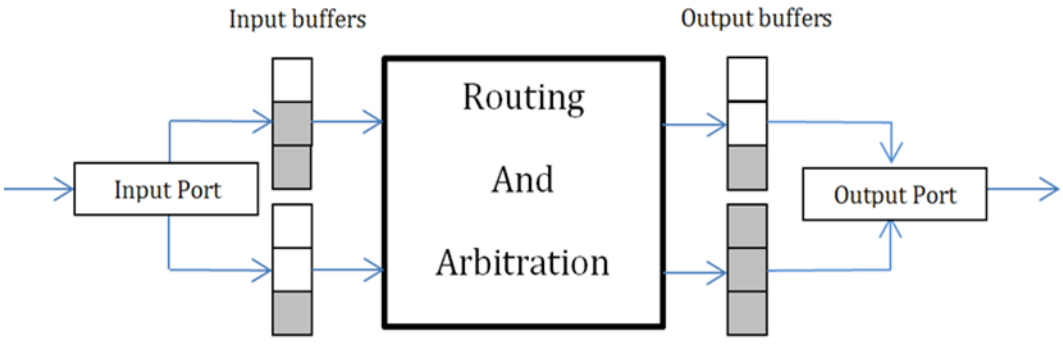

Figure 1-2 NoC switch architecture

Thus a virtual channel is available for the packets that are blocked. The header flit will be dropped if all the virtual channels are occupied. The source will have to send the header flit again in this case. Fig. 1-2 shows the architecture of a switch in NoC.

1.4 Emerging interconnects

The Interconnects uses dielectric wires to transfer data. But as the wires are getting thinner and thinner, resistance of the wire increases. The increase in resistance in turn increases the wire delay and heat dissipation. The bandwidth offered by the planar dielectric wires is also less. With increase in number of cores, large number of parallel buses has to be laid. This makes the scalability with dielectric wires, in terms of number of cores not possible. According to the International Technology Roadmap for Semiconductors (ITRS) interconnects are the major bottlenecks to overcome the power-performance barrier in the future generations. Hence, there is a need for scalable interconnect system.

Some of the new interconnect technologies such as 3D integration, wireless interconnects, and photonic interconnects are being explored. These alternative interconnect technologies are predicted to support multi-core chips.

Three-dimensional (3D) integration consists of multiple layers of chips, stacked one above the other. The chips are connected through vertical vias. The major advantage of 3-D ICs is the reduction in length and number of global interconnects, which leads to increase in performance and decrease in power consumption [5]. It also allows connecting two different technologies with each other. Disadvantages of 3D chips are that they harder to manufacture as the layers of chips should be

aligned properly. Any misalignment in the vias will make the chip useless. Also, due to their smaller surface area, dissipation of heat becomes a problem.

In wireless interconnects, global interconnects are replaced by single-hop long-range wireless shortcuts operating in the millimeter (mm)-wave frequency range. The recent studies in wireless interconnects have lead to several architectures that can provide low latency, better power consumption [6]. But, the failures during fabrication of carbon nano tube antennas (CNT) are much higher than CMOS process. The electrical characteristics of the CNT are difficult to control. This leads to failure of links, shadowing the advantages of wireless links.

In optical interconnects, the packets are transmitted in form of light. A serial bit stream of packet, in electrical form is presented to the modulator and the bit stream will be encoded for data transmission in optical fiber. The encoded packet from the modulator will drive the light source. The on-chip laser is the light source for the photonic packets. The light wave will reach the photo-detector after incurring losses at the optical fiber. The packet in the optical domain will be converted into electrical domain at the photo-detector.

The optical fiber can support multiple wavelengths inside it. Hence, Wavelength Division Multiplexing (WDM) is used in the optical interconnects to increase the data bandwidth. The light can travel much faster inside an optical fiber than packets in dielectric interconnect. The performance of photonic elements is improved frequently through research. This facilitates the design of low latency, high bandwidth interconnects. However, designing interconnect network for high

reliability is a non-trivial challenge. The network architecture of the photonic interconnects determines the reliability of the packet.

The length of the optic fibers, number of bends, number of MRRs on the path of the packet, and number of wavelengths used for WDM determines the signal loss incurred by the packet. Using segmented waveguides instead of long waveguides will alleviate the signal loss problem. The segmented waveguides facilitate scalability of network architecture, in number of cores, without degradation in reliability.

1.5 Thesis Contribution

In this thesis work, the performance and reliability of different PNoCs will be studied. A non-blocking MSB (NMSB) PNoC, with better performance will be proposed. It will be demonstrated that the NMSB photonic NoC (PNoC) has better latency, low packet energy, and high bandwidth over other PNoCs. The reliability of different PNoCs will be studied.

The following point summarizes the contributions made during this work.

- **Proposed Network Architecture**

  A non-blocking segmented bus PNoC called NMSB is proposed.

- **Reliability analysis**

  Worst case reliability analysis of different PNoCs.

- **Experimental results**

- Develop a cycle accurate simulator to implement the wireless NoC architectures with 3-stage switches namely, input, output arbitrations and routing to determine the following parameters
- Develop a BER analysis model to evaluate the reliability of different PNoCs using the signal losses incurred by the packet.
- Obtain experimental results of the proposed NMSB PNoC architecture with other electronic and photonic NoC architectures with respect to the following parameters using the cycle accurate simulator
  - Peak achievable bandwidth
  - Packet energy dissipation
  - Non-uniform traffic patterns
  - Area overheads
  - BER

➢ **Publications**

- Pradheep Khanna Kaliraj, Patrick Sieber, Dr. Amlan Ganguly, Ipshita Datta, Dr. Debasish Datta. "Performance Evaluation of Reliability Aware Photonic Network-on-Chip Architectures" International Green Computing Conference 2012 in San Jose, CA.

- Pradheep Khanna Kaliraj, Amlan Ganguly, "Trade-offs in Reliability and Performance of Photonic Network-on-Chip Architectures". Submitted in IEEE Transaction on computers. August 2013.

Chapter 2 Related Work

Recent advances in the nano-scale fabrication and dense integration of silicon devices have led to the development of photonic devices that can be integrated on the multi-core chips. Conversion of electronic signals to optical signals and vice versa had been made possible on the multi-core chips with the on chip photonic elements such as micro-ring resonators. Ability to lay down multiple photonic waveguides on the surface of the multi-core chips has made novel PNoC architectures feasible. Several high-performance and low-energy PNoC architectures have been proposed in existing literature. The architecture of the PNoCs and the photonic elements used in the study are given below.

2.1 Photonic Elements

The Micro Ring Resonators (MRR), on-chip laser source and photonic waveguides are the important photonic elements on the PNoC that enable electro-optic conversion of data and photonic communication. The electrical packet generated by the core will be converted to optical packet of certain wavelength by the MRR modulators. The light source for the photonic packet is provided by the on chip laser source. Optical fibers are used as a medium to carry the photonic packets. The PNoC uses WDM to increase the bandwidth of the links. An array of MRRs is used in the waveguides to modulate and filter different wavelengths.

2.1.1 Micro ring resonator

The micro ring resonators are used for modulating, filtering, and routing the light waves on the PNoC. MRRs should be small in size, capable of modulating the light signals at high speed, and consume less energy. Today, the MRRs are as small as 4um in diameter and with a free spectral range of 6.92 THz [7]. These MRRs can modulate a light signal at a speed of 12.5 Gb/s. The adiabatic micro ring modulators are able to meet the requirements of the PNoC architectures than the older mach-zehnder modulator (MZM) [7]. This is because the adiabatic MRR has better power consumption and lesser resistance than the MZMs. The adiabatic transition from wide, multimode contact to narrow, single mode contact eliminates unwanted spatial modes. The single mode coupling and lesser resistance in the adiabatic MRRs increases the speed of operation. The light waves will be coupled on to the MRR only when the wavelength of the light matches with the resonant frequency of the MRR. The resonant frequency of the MRR can be changed by applying heat to them. The heat is applied on the MRR with the help of local heaters. We assume a single heater element per MRR in the PNoCs enabling the thermal tuning.

The light wave travelling along the waveguide gets coupled with the particular MRR, which has the resonant frequency. Light waves of other frequencies will not be affected by that modulator. An array of MRRs and heaters is used to modulate and filter the light waves at the source and destination respectively when WDM is used. A heater

associated with the MRRs will be used to tune the MRRs to the certain frequency in which the photonic packet should be modulated.

2.1.2 Photo-detector

The demodulation is done with the help of on-chip photo-detectors. In PNoCs where WDM is used the MRRs are used along with the photo detectors. The MRRs at the destination act as frequency filters. The MRRs tuned to particular frequency will get the corresponding light waves to the photo detector, where the light signal will be converted back into electrical signals. The on-chip photo detector parameters such as photo-detection threshold, power consumption, and bit rate play an important role in governing the efficiency of the PNoC. Germanium photo-detectors of size 0.7umx20um have been demonstrated to operate at 40 Gbps [7]. The photo detector responsivity as high as 0.74A/W has been demonstrated [9].

2.1.3 Switches

Photonic switches are made up of MRRs. Some PNoCs require light waves to be turned by 90^0. One such PNoC is 2Dimensional Folded Torus (2DFT) PNoC [10]. For every packet, an electronic header flit sets up the path for the photonic body flits. The header flit uses dimension order routing along an electronic mesh to setup the path [10]. Hence, the photonic body flits needs 90^O turns to reach the destination. A 2x2 photonic switch is shown in fig. 2-1. The electrical header flits have intermediate addresses of the nodes where the photonic packets should take a 90^0 turn. The photonic switches associated with these nodes will be setup to turn the photonic packets.

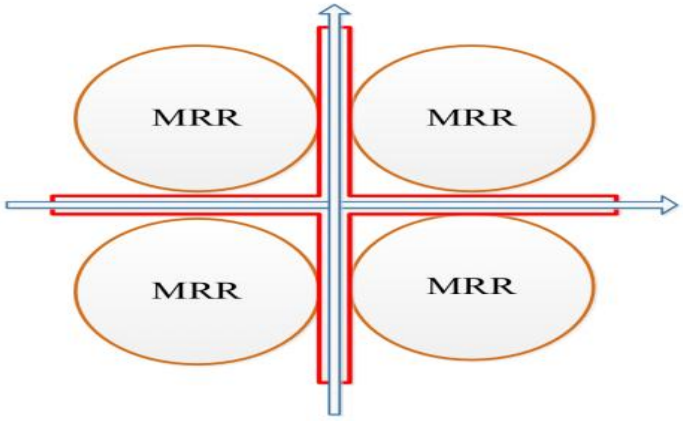

Figure 2-1 A basic photonic switch

The heaters associated with the MRRs are used to tune the MRRs into resonance frequency. A MRR is said to be ON when the resonant frequency of the MRR matches the frequency of light wave to be turned by 90^0. The photonic packet couple with the MRR which is ON, thus making the 90^o turns. The photonic packet will simply pass through the switch if all the MRRs in the OFF state. A non-blocking photonic switch using MRRs as building blocks has been demonstrated in [10].

2.1.4 On-Chip Laser Diode

A small foot-print, multiple wavelength laser sources are required for the PNoC. The laser source should operate with low threshold currents. Micro-disk lasers operating in continuous-wave regime at room temperature, with a threshold current of 0.9 mA and a waveguide-coupled slope efficiency of up to 8 W/mA is demonstrated with a micro-

disk diameter of 7.5µm[8]. Multi-wavelength laser source heterogeneously integrated with silicon-on–insulator waveguide circuit has been demonstrated in [8].

2.1.5 Optical waveguides and couplers

The on-chip optical waveguides are similar to the conventional optical fibers that carry long distance optical signals. On-chip waveguide consists of core surrounded by cladding. The core and cladding is made of materials whose refractive index is significantly different. The difference in the refractive index between the core and cladding confines the signal inside the core by total internal reflection. The optical signal undergoes multiple reflections inside the core while moving along the waveguide. In PNoC, silicon wire waveguide on silicon on insulator is used as the carrying medium for the optical packets. The output from the laser diode should be coupled efficiently with the silicon waveguide for low power consumption [8]. With flip-chip bonding of GaInNAs/GaAs, laser diodes can be directly coupled on to silicon substrate. Spot-size converters are used to couple the laser light from laser diode to silicon waveguide. For single wavelength operation, photo-detectors can be directly integrated with the silicon waveguide. A complete optical transmission link, which has a single silicon waveguide integrated with both laser diode and photo-detector, is demonstrated in [8].

2.2 Existing PNoC Architectures

The PNoCs in existing literature that are used in the study are 2DFT PNoC, Clos PNoC [12] and Corona PNoC [13].

2.2.1 2DFT PNoC

The 2DFT is a hybrid NoC which uses a hybrid electronic and photonic NoC to transmit data. The photonic paths to be used by body flits are laid out by electronic control headers by turning on or off photonic switching elements. The photonic interconnections in the 2DFT PNoC consist of a torus rings along with special switches such as Insertion Switch (IS), Network Switch (NS), Gateway Switch (GS), and Ejection switch (ES). A 4 cluster 2 DFT Architecture is shown in fig. 2-2. The packets are injected from the GS. Each cluster has a single GS associated with it. The packets are generated through GS from the clusters. GS contains the modulator and demodulator MRRs. The IS injects the packet generated by the GS into the network. The Network switches (NS) turn the photonic packet towards the destination. The final switch before the packet reaches the destination cluster is the Ejection switch (ES). The ES will be in the adjacent column, but on the same row as that of the gateway switch. The packet makes its final turn on this switch to reach the GS. The Header flit which is an electronic packet has the intermediate addresses for the IS, NS, and ES, the packet should be affected. The Electronic router sets up the path for the following photonic packet. The electronic header flit flows through the electronic path and sets up the MRRs for photonic switching. The photonic- Electronic conversion will only take place in the destination cluster. The photonic packet simply flows through the path laid by the electronic header flit. The Gateway switch injects the header flit into network. The Electronic header flit will be routed through the switches. The header flit will be stored in the buffers if the link is occupied for other data transfers. Also, the number of packets that can be inserted

into the architecture depends on the number of IS available in the network. With PM = 1, there will be 64 IS present inside the PNoC. Hence, only 64 out of ${}^{64}C_2 \times 2 = 4032$ connections are possible inside this PNoC. The performance of the 2DFT architecture increases by increasing the path multiplicity of torus rings. The increase in path multiplicity of the torus rings increases the number of links available in the PNoC. The number of IS in the PNoC increases directly with the increase in PM. The complexity of the PNoC also increases with the increase in Path multiplicity. But the performance does not increase drastically after the path multiplicity of 2 [10]. The 2DFT uses WDM with 24 wavelengths. The 24 wavelengths are used by a single packet from one cluster [10].

2.2.2 Clos PNoC

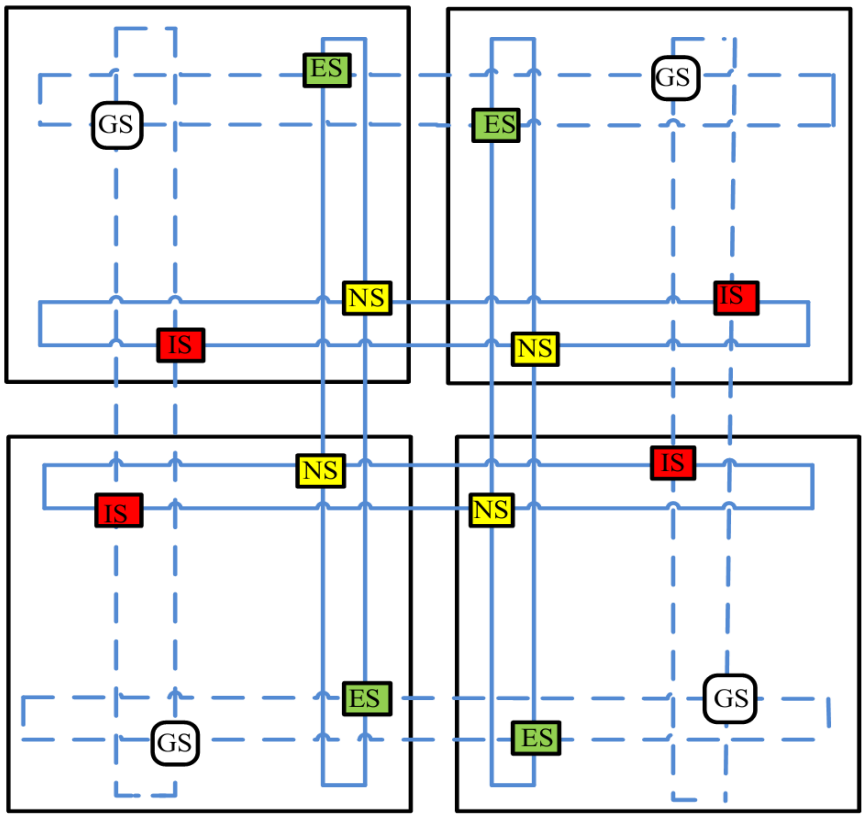

Figure 2-2 A 4 Cluster 2DFT PNoC

CLOS PNOC [12] uses 8x8 electronic cross-bars along with photonic links to transfer data between 64 clusters. Clos PNoC consists of 8 clusters grouped into one tile. Every tile has its own router to communicate with the other tiles. The eight clusters in a tile are connected to each other through electronic links. The communication between tiles takes place through hybrid links consisting of both photonic and electronic links.

The inter tile communication takes place through multiple hops. The packet undergoes an electronic-optical conversion at each hop along the inter-tile communication. Three electronic routers are used in the process of inter tile communication.

The cluster in a tile will send the packet through electronic link to the first router. The router will forward the packet to the second router as a photonic packet in one of the available 64 wavelengths. The second router again converts the Photonic packet into electronic packet, so that it can be processed in the router. The third router receives the photonic packet and converts it into electronic packet and forwards it to the appropriate destination after processing the electronic packet. Fig. 2-3 shows an example of inter-tile communication in CLOS PNoC architecture.

There are $64C2 \times 2 = 4032$ connections present in the architecture. Out of 4032 connections, there are $8C2 \times 8 = 448$ intra tile connections. Rest of the connections are inter tile connections which uses three electronic router and two Electronic-Optical and Optical-Electronic conversions. Hence in a 64 cluster CLOS PNoC, 89% of the total communication is inter-tile communication. This is made possible with the

use of 56 optical waveguides, each with 64 wavelengths within them through DWDM.

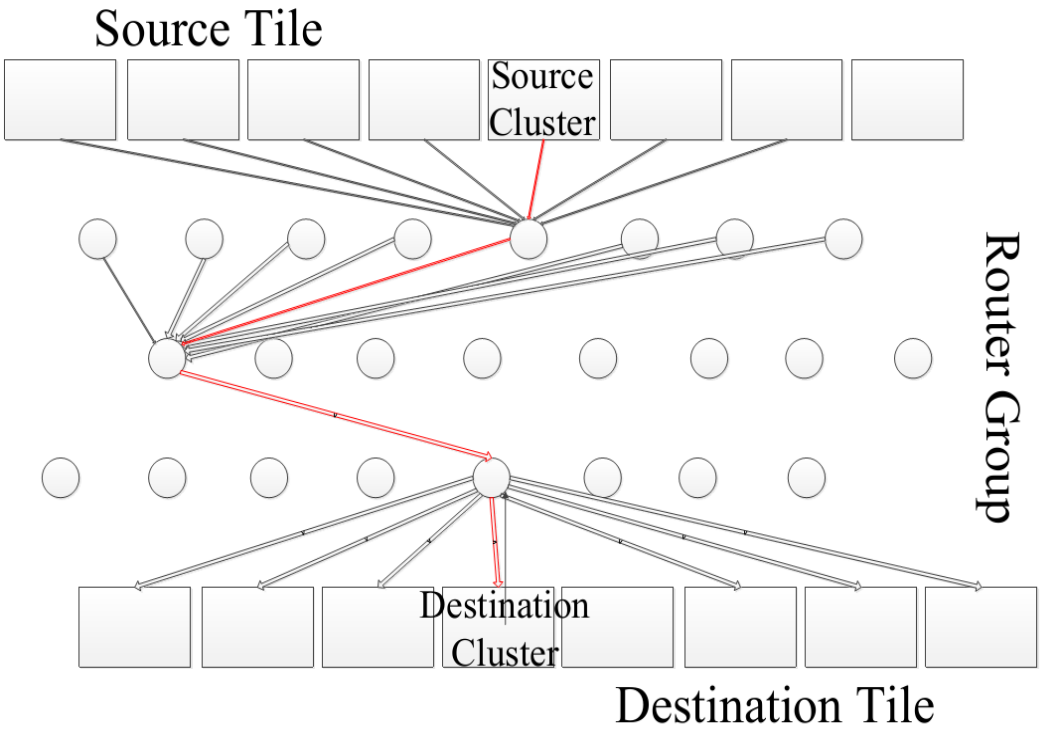

Figure 2-3 Inter-tile communication in Clos PNoC

2.2.3 Corona PNoC

Corona is an all Photonic PNoC which provides one to one connection to all clusters present in the architecture. A waveguide originating from a given cluster traverses through all the clusters in the PNoC architecture and terminates at the originating cluster. There are N waveguides in 'N' cluster corona PNoC architecture. A packet inserted into the network has to pass through large number of MRRs before reaching the destination. 4 cluster corona PNoC architecture is shown in fig 2-4. Corona uses dense wavelength division multiplexing (DWDM).

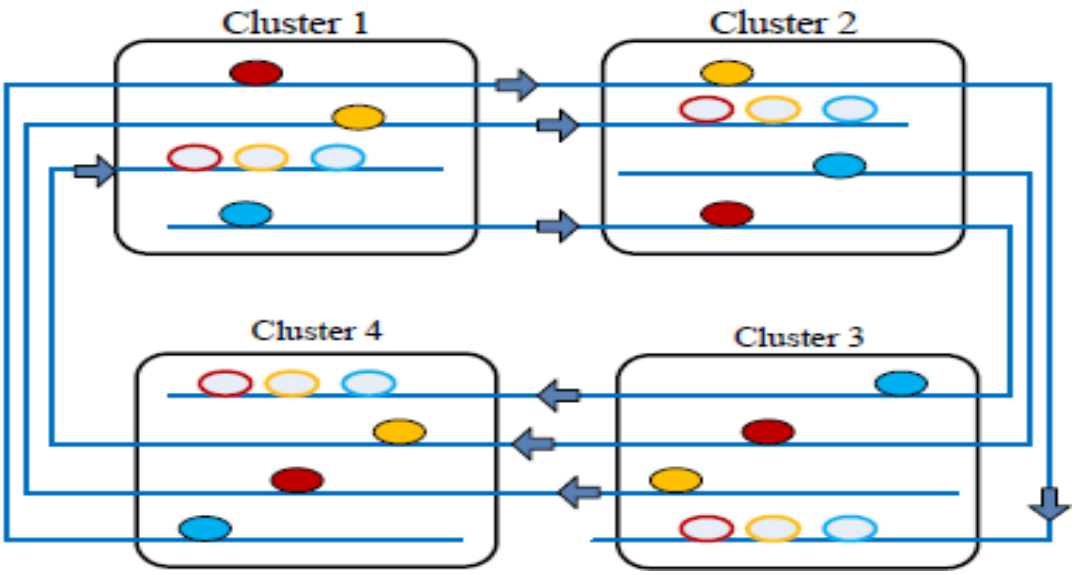

Figure 2-4 4 Cluster Corona PNoC

A waveguide can support up to 62 wavelengths with $\Delta\lambda$ = 0.8nm in 50 nm WDM bandwidth. The Corona PNoC can only support only single wavelength per link in a 64 cluster architecture. The number of waveguides should be doubled in order to increase the link speed. But with the increase in number of waveguides, number of MRRs associated with them increases.

The photonic packets generated from the source cluster will be sent to the destination cluster in a single hop, with the help of dedicated links. The photonic packets will be stored in the buffers once they undergo photonic to electronic conversion. There is no problem of path setup packet, the header flit, being dropped or lost, since every other cluster has a one to one connection.

Extending Corona PNoC architecture for clusters more than 64 cluster architecture will not be feasible with the current technologies. The packets will have

to traverse a long path and pass through more MRRs with increase in the number of clusters. This will have adverse effects on reliability of packet sent.

Chapter 3 Network Architecture

From the existing architecture, we understand that, the long optical waveguides, large number of MRRs on the path, and multiple wavelengths affect the reliability of the packet transferred. Also, the existing PNoCs cannot be scaled up to accommodate more number of clusters without considerable loss in reliability. Hence, architecture is proposed here that can provide competitive performance without affecting the reliability.

3.1 Multiple Segmented Bus PNoC

The architecture of the MSB-PNoC is designed for reliable on-chip data transfer through the photonic interconnects. The number of MRRs on a waveguide, the length of waveguide and the number of waveguide bends are the major components that cause signal power degradation along the waveguide. Crosstalk interference due to WDM is another reason for loss of reliability. Due to the reliability aware design of the MSB PNoC, number of MRRs in a waveguide and the length of the waveguide are restricted to achieve better bit error rates (BER). The number of wavelengths to enable DWDM in a given waveguide is limited in the MSB-PNOC. Consequently, the interference noise due to adjacent channel crosstalk is also limited. But the performance of the MSB-PNoC is affected by the reliability aware design. Hence, the NMSB PNoC architecture is proposed here, which is primarily a MSB PNoC along with non-blocking architecture to improve the performance without affecting the reliability. The topology and communication protocol of the MSB PNoC and NMSB PNoC are discussed in this section.

3.2 Scalable Topology

Packets from the clusters are sent to their destinations through segmented waveguides in the MSB PNoC. The segmented waveguides facilitate scaling of number of clusters or cores in MSB PNoC without degradation in reliability. A 16 cluster MSB-PNoC is shown in fig. 3-1.

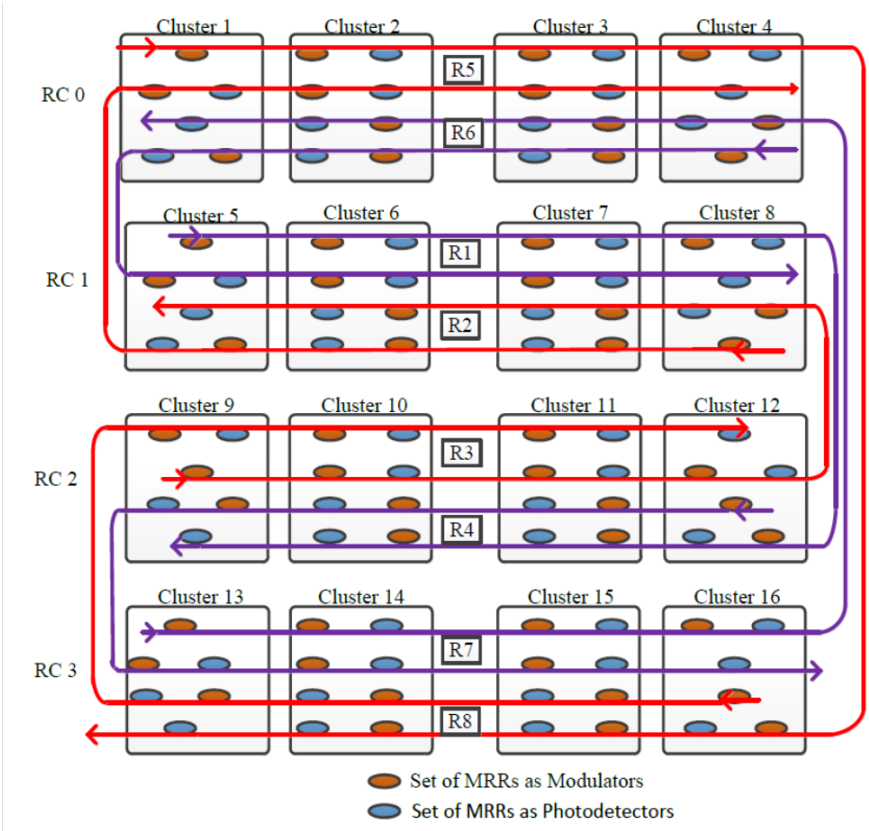

Figure 3-1 A 16 Cluster MSB PNoC

Waveguides of the 16 cluster MSB PNoC are segmented such that a single waveguide traverses exactly 8 clusters. In this way, the number of MRRs along the waveguides and the lengths of this type of waveguides are same throughout the PNoC. Segmented buses traverse from the source row cluster RC(m) to destination row cluster RC(n), where $m, n \epsilon \{0,1, \ldots . log_2(N) - 1\}$ for a N cluster architecture.

The vertically adjacent rows such as RC(0)-RC(1), RC(1)-RC(2), RC(2)-RC(3), and RC(3)-RC(0) are connected by segmented buses in both clockwise and anti-clockwise direction. Hence, there are two segmented buses running between any two RCs. The connectivity is given by

$$RC\ (i[mod - N]) - RC(i + 1[mod - n]) \quad (1)$$

The vertically adjacent rows of clusters in a 16 cluster MSB PNoC communicate with each other using just one segmented bus and it is referred as a direct connection. While, vertically non adjacent row clusters, communicate with each other using two segmented buses and it is referred as indirect connection. Fig. 3-2 shows an example for both direct and indirect connections. A direct connection, shown in blue dotted lines, is established between cluster 5 and cluster 9, since they are in rows vertically adjacent to each other. The cluster 1 and 10 that are placed in vertically non adjacent rows are connected through an indirect connection shown in green dotted lines. RC (0) and RC (2) are connected with the ISR R8 as shown in fig. 3-2. The vertically non-adjacent row clusters are connected through two segmented waveguides with the help of Inter Segment Routers (ISR). Each ISR is made up of two photonic switches adjacent to each other and connected by a waveguide. Each photonic switch provides a 90^0 bend to the photonic signal. The ISRs tuned to certain frequency to switch photonic packets between waveguides. They switch a photonic packet of given wavelength from one segmented bus to another bus in the same direction which is running parallel to it.

In an indirect connection, only two of the clusters in the non-adjacent row are connected to the given row in one direction. A different set of waveguides is

used to connect other two clusters of the row. This is shown in fig.3-2, where the indirect connection (green dotted line) terminates at cluster 10 even when the waveguide runs up to cluster 12. In this case to connect cluster 1 with cluster 12 or

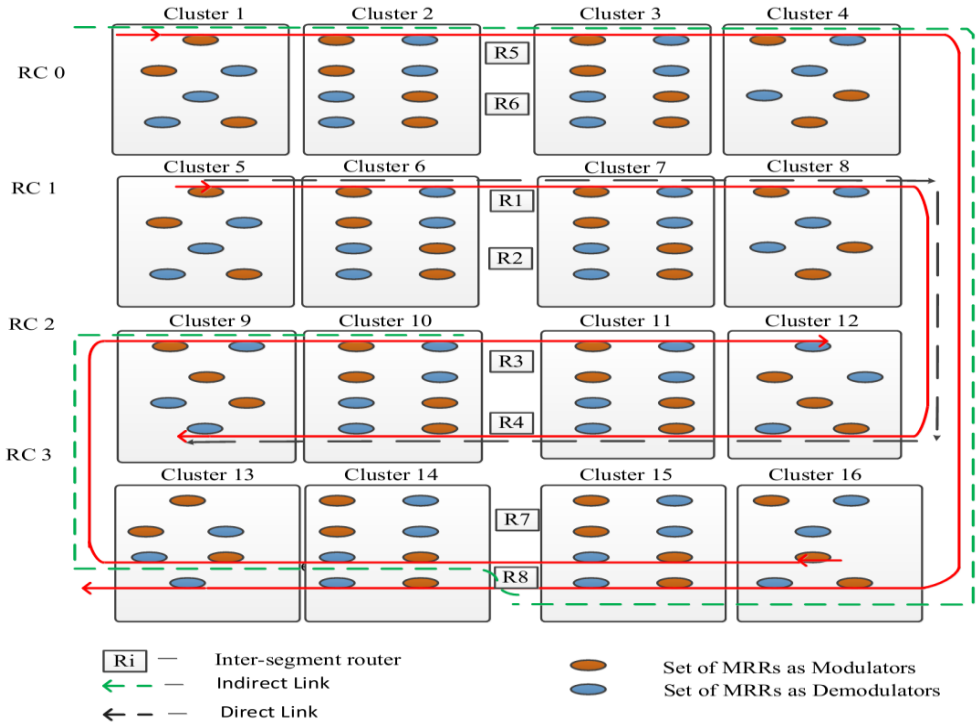

Figure 3-2 Direct and Indirect links in a super cluster.

cluster 11, the waveguides through RC(0), RC(1) and RC(2) will be used. Thus the maximum distance that photonic packets travel through waveguides and the number of clusters on its paths is limited. This approach minimizes the signal loss incurred due to waveguide loss, MRR insertion loss, and crosstalk interference.

The MSB PNoC can be scaled up into architectures with higher number of clusters, without any drastic adverse effect on the reliability. 64 cluster MSB PNoC architecture is built by connecting four 16 cluster MSB PNoC architectures through a set of Inter Group Buses (IGB). The 16 cluster MSB PNoCs in 64 clusters system will be referred to as *superclusters*. A pair of IGB runs between the superclusters in

opposite direction. The 64 cluster architecture is shown in fig. 3-3. IGBs are connected to RC (3) of the two top superclusters and RC (0) of two bottom super clusters. The Row clusters that are connected to the IGBs are called “Gateway Clusters” (GC). These GCs are directly connected to each other by the IGBs and they are used as intermediate cluster for communications between super clusters. The factors that affect the reliability of the signal in a waveguide such as, the number of MRRs, waveguide bends and crosstalk are less in the IGBs compared to the segmented busses within a super cluster as discussed in section 4.3 and 4.4. Hence, the reliability of photonic data transfer is not degraded due to the IGBs enabling scaling up the system size.

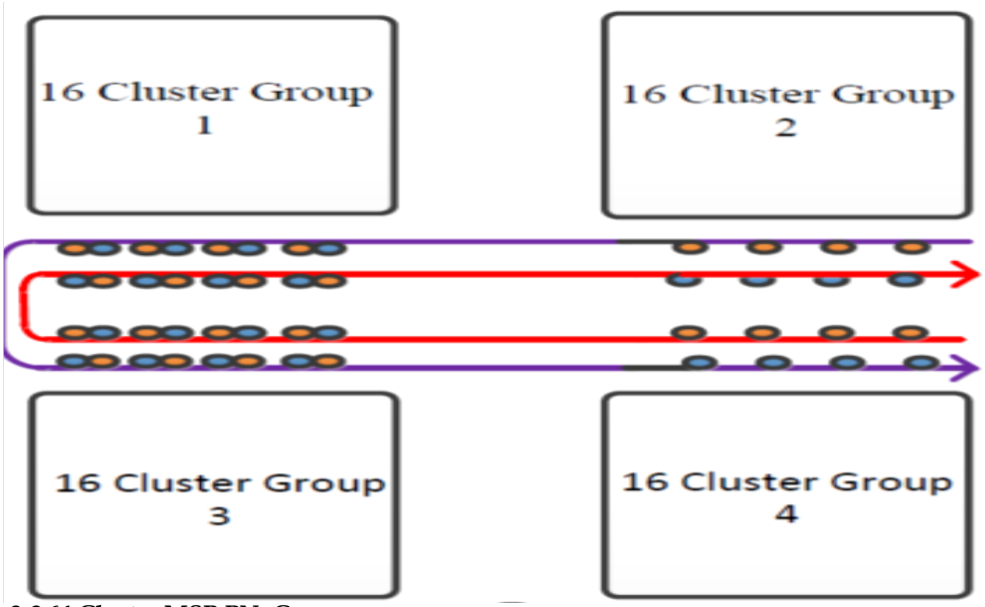

Figure 3-3 64 Cluster MSB PNoC

3.3 Communication Protocol

The MSB is an all-photonic NoC architecture. It uses wormhole routing to transfer data from the source to destination cluster. In 64 clusters MSB PNoC

architecture, data is transmitted from source to destination cluster in multiple hops. In a multi-hop link, the header flit goes through Electro-Optic (E-O) conversion at each hop and is stored in the electronic buffers before it is converted into the optical packet and sent to next cluster. But within a 16 cluster MSB PNoC all the communication is single-hop without the need for any intermediate E-O conversion. The communication between super clusters takes place through IGBs. The cluster in RC (m) sends data to GC through one of its segmented waveguides. Once in GC, the data will undergo optical-electrical-optical (O-E-O) conversion and transmitted to a GC of super cluster, which contains the destination cluster through IGB. Once in the receiving GC, the data again undergoes O-E-O conversion and it will be sent to destination cluster using the segmented busses.

3.4 Wavelength Assignment

The wavelengths are equally distributed along the waveguides of same type in order to have same crosstalk and MRR distribution throughout the PNoC architecture. The unidirectional waveguide SB_{mn} in the MSB traverses through eight clusters in two rows. With SB_{mn}, the clusters in row *m* can send data to clusters in row *n* and the clusters in row *n* can send data to the clusters in same row *n*.

Within a 16 cluster MSB architecture there are 240 (16 x 15) connections. Each of the 16 clusters in a super cluster will communicate with 15 other clusters. Every cluster inside the 16 cluster architecture has a one to one connection between other clusters. Within a single segmented bus SB_{mn}, there will be 38 wavelengths. Out of 38 wavelengths, 22 wavelengths will be used for the direct connections and 16

wavelengths will be used for the indirect connections, which are achieved through ISRs.

The speed of the links can be doubled by doubling the number of wavelengths between source and cluster. In this case, there will be 76 wavelengths per waveguide in the PNoC. But, 76 wavelengths cannot be supported in a single waveguide due to crosstalk noise. The maximum number of wavelengths that can be supported in a waveguide is 62 with DWDM [14] . In order to reduce the number of wavelengths in a waveguide; compromise is made on the speed of the links. Hence, in a MSB PNoC, some links operate with two wavelengths, whereas others will be operating with single wavelength. Each cluster inside a super cluster will have to communicate with four other clusters through indirect link. Hence, inside a super cluster, the 64 indirect links, the one which uses ISR to reach the destination will be a single wavelength link and the rest 176 direct links can have two wavelengths between them. In this case, the number of wavelengths inside a waveguide will be confined to 60 (22 x 2 direct links+ 16 indirect links).

3.5 Non- Blocking MSB Architecture

From section 4.2 we can see that in a MSB PNoC, both inter cluster and intra cluster communication takes place through the segmented waveguides SB_{mn} and $SB_{nm.}$ Hence, the photonic packets which need to travel outside a super cluster have to contend for the available links for packet transfer with those that don't need to. Photonic packets will be stalled or dropped due to this blocking nature of the MSB-PNoC, affecting the performance. In the non-blocking NMSB PNoC, special

waveguide buses are used for inter super-cluster communication. These special segmented buses introduce more links between clusters for inter super-cluster communication.

A complete 16 cluster NMSB architecture is shown in fig. 3-4. Three RCs in super clusters are directly connected to GC by special segmented bus SB_{mg} and vice versa, where 'm' is the source row cluster and 'g' is the Gateway row cluster. These sets of special segmented buses are used by the RCs for communication between super clusters only.

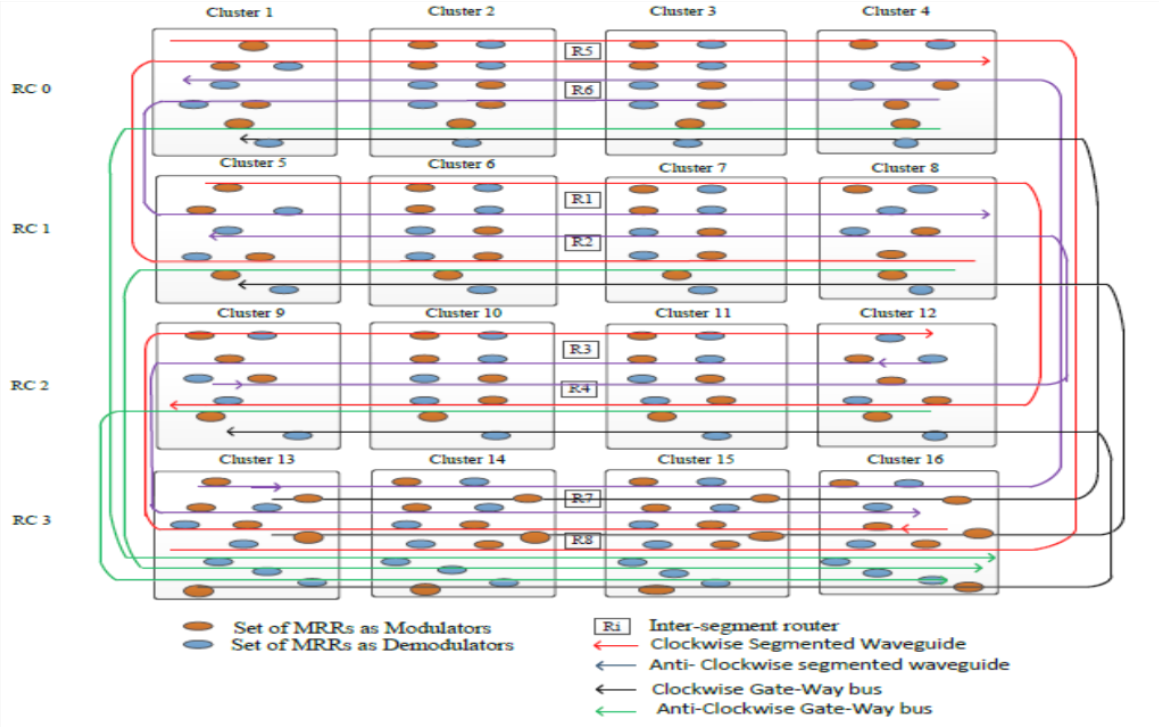

Figure 3-4 A 16 Cluster NMSB PNoC.

Since there are 48 clusters outside any given super cluster for a 64 cluster system, every cluster will need 48 wavelengths to communicate with destination clusters in

other super clusters. These 48 wavelengths will be routed to the gate way clusters and from there to destination clusters through inter group buses (IGB). There are 4 SB_{mg} and SB_{gm} segmented buses in every row, one for each cluster, except the gate-way row cluster. SB_{mg} and SB_{gm} run in opposite directions with a single WDM channel per link. Each row cluster will require 192 (4 x 48) wavelengths to send data from four of its clusters to the gateway clusters. Since all 192 wavelengths cannot be supported in a waveguide, we propose distributing these wavelengths into 4 waveguides resulting in a PM of 4 for every SB_{mg} and SB_{gm}. There are 48 wavelengths in each SB_{mg} and SB_{gm} and the buses traverses through 8 clusters. Hence, the reliability of the SB_{mg} and SB_{gm} busses is better than the other segmented busses within a supercluster due to lower crosstalk as they support less number of WDM channels. The intergroup buses should be able to support all communications between 64 clusters. Each of the 16 clusters in a super cluster, communicates with 48 other clusters located in other super clusters forming 768 inter super-cluster links from each. Hence the IGB has to support 768 wavelengths for every super-cluster with single channel connections. Therefore, PM of 32 on IGB pair is used to support such large number of wavelengths. In this way each IGB will have 48 wavelengths satisfying the maximum limit on WDM on each waveguide. The Super cluster where the IGB originates will have 24 wavelengths; immediate super clusters will have 16 and 8 wavelengths to send data on each IGB. Hence there will be a total of 64 IGBs in total with 48 wavelengths and 96 MRRs on each one of them.

The PM of IGBs, SB_{mg}, and SB_{gm} should be increased in order to increase the performance of 64 cluster architecture. The area overhead increases due to increase

in number of waveguides and MRRs associated with these waveguides. This also leads to the signal loss due to more number of MRRs on the path of packet. Hence, to strike a balance between performance and area, the IGBs, SB_{mg}, SB_{gm} will have single channel links between source and destination. This reduces the number of IGBs, SB_{mg}s, and SB_{gm}s used in the PNoC. In the 64 cluster MSB PNoC there will be a PM of 64, 4, and 4 for IGBs, SB_{mg}s, and SB_{gm}s respectively. These modifications to the MSB PNoC enables the non-blocking architecture referred to as NMSB.

Chapter 4 Reliability Analysis

A methodology for analysis of the reliability of photonic data sent across the 64 cluster PNoC is developed for different architectures in this section. The losses incurred by the photonic packet along the waveguide such as waveguide loss, bending loss, MRR pass through loss and crosstalk loss leads to degradation of power in the data sent. The signal losses in db, due to different sources are given in table 4-1 [15]. The various data used in the analysis are photo-detector responsivity (R_λ), defined as the measure of electrical output with respect to optical input. It is expressed in amperes per watt R_λ = 0.75A/W; MRR modulator extinction ratio is defined as the ratio of the energy used to transmit a logic level '1', to the energy used to transmit a logic level '0'. Extinction ratio is considered to be-15dB/-0.1dB (for binary 0/1 transmission) in our experiment and receiver transimpedance is 316Ω. DWDM is used in these PNoCs with Δλ (space between adjacent wavelengths) = ~0.8 in 50nm WDM bandwidth [14]. The loss across a link differs between the topologies because of their inherent architectures.

Source	**Loss in db**
Waveguide loss	2db/cm
MRR pass-through loss	0.005dB
Waveguide bending loss	$0.005dB/90^0$

Table 4-1 Losses in Optical path [15]

To determine the worst case BER of a given topology, the longest link between two nodes are taken and the losses along the path are calculated. The losses

accumulated together with the crosstalk-induced interference are then used to find the worst case BER of the PNoCs.

4.1 Bit Error Rate Model

In this section, we present an exhaustive BER evaluation model which is applicable to all possible interconnect topologies, with varying degree of losses and crosstalk interference, governed by the topology under consideration [16]. We consider a pair of clusters located at a distance from each other, having inter-cluster light wave communication between two cores, each core taken from one of the two given clusters. The light wave received at the destination cluster in presence of crosstalk is expressed as:

$$\mathrm{E_R(t)} = \sqrt{(2\mathrm{P_s(b_i)})}\cos(\,2\pi \mathrm{f_s t} + \theta_\mathrm{s} + \phi_\mathrm{s}(\mathrm{t})) + \mathrm{E_{XT}(t)} \qquad (2)$$

The first term on the right hand side of equation (2) describes the signal component received at the destination cluster, $P_s(b_i)$ is the bit dependent received signal power taking into account all the losses along the pathway, where $b_i \epsilon \{0, 1\}$, f_s is the signal frequency, θ_s is the initial phase and $\phi_s(t)$ is the phase noise of the signal component of the lightwave. $E_{XT}(t)$ defines the accumulated crosstalk component given by

$$E_{XT}(t) = \Sigma_{j=1}^{W}\sqrt{(2P_{xj})}\cos(\,2\pi f_j t + \theta_j + \phi_j(t)) \qquad (3)$$

Where W represents the number of crosstalk components, P_{xj} is the received power of the j^{th} crosstalk component, f_j is the frequency of the j^{th} crosstalk component, θ_j and $\phi_j(t)$ are the initial phase and phase noise of the j^{th} crosstalk component. The photocurrent produced at the photo detector output is expressed as

$$i_p(t) = R_\lambda < {E_R}^2(t) > + i_{th}(t) + i_{sh}(t) \quad (4)$$

The first term on the right hand side of equation (4) defines the *square-and-average* operation of the photo detector on the received light wave, with R_λ as the photo detector responsivity, the second term is the thermal noise of the receiver and the third term represents the signal dependent shot noise. The first term of the right hand side of equation (4) can be expressed as

$$R_\lambda < {E_R}^2(t) > = \ i_s(t) + i_{sx}(t) + i_{xx}(t) \quad (5)$$

Where, $i_s(t)$ is the signal component of the photocurrent, $i_{sx}(t)\ and\ i_{xx}(t)$ represent the crosstalk-crosstalk and signal-crosstalk beat noise components. We express $i_s(t), i_{xx}(t)\ and\ i_{sx}(t)$ as

$$i_s(t) = R_\lambda P_s(b_i) \quad (6)$$

$$\mathrm{i_{xx}(t)} = \mathrm{R_\lambda[}\ \Sigma_{j=1}^{W} P_{xj} + \Sigma_{j=1}^{W}\Sigma_{k=1}^{W}\sqrt{(P_{xj}P_{xk})}\cos(\omega_{jk}t + \phi_j(t) - \phi_k(t) + \theta_j - \theta_k) \quad (7)$$

$$i_{sx}(t) = \ 2R_\lambda\Sigma_{j=1}^{W}\sqrt{(P_s(b_i)P_{xj})}\cos(\omega_{js}t + \phi_j(t) - \phi_s(t) + \ \theta_s - \theta_j) \quad (8)$$

where, $\omega_{js} = \omega_j - \omega_s$ and $\omega_{jk} = \omega_j - \omega_k$ represent the respective beat-noise frequencies.

The combined electrical noise(shot noise, thermal noise and signal-crosstalk beat noise (crosstalk-crosstalk beat noise ignored)) after photo detection is modeled as a zero-mean Gaussian random process with the variance expressed as

$${\sigma_{bi}}^2 = {\sigma_{sxi}}^2 + {\sigma_{shi}}^2 + {\sigma_{th}}^2 \quad (9)$$

Where, ${\sigma_{th}}^2$ is the thermal noise variance with R as the input impedance, B_e as the noise equivalent bandwidth of the optical receiver , k as Boltzman‟s constant, T as receiver temperature and ${\sigma_{shi}}^2$ represents the shot noise variance, given by

$${\sigma_{th}}^2 = (4kTB_e)/R \tag{10}$$

$${\sigma_{shi}}^2 = 2q[R_\lambda P_s(b_i) + R_\lambda \Sigma_{j=1}^{W} P_{xj}]B_e \tag{11}$$

and the worst-case signal-crosstalk beat noise variance ${\sigma_{sxi}}^2$ is:

$${\sigma_{sxi}}^2 = {R_\lambda}^2 \Sigma_{j=1}^{W} P_{xj} P_s(b_i) \tag{12}$$

The receiver BER can be evaluated as

$$BER = P(1)P(0/1) + P(0)P(1/0) \tag{13}$$

Where, P(0) and P(1) are the transmission probabilities of ‘0’ and ‘1’ and, P(1/0) and P(0/1) are the respective conditional error probabilities. Under the Gaussian assumption for the probability density functions, the BER can be expressed as [16]

$$BER = 0.5erfc(Q/\sqrt{2}) \tag{14}$$

where, $Q = R_\lambda[P_s(1) - P_s(0)]/(\sigma_1 + \sigma_0)$ and the noise variances for the bits$\{b_i\}$ are given by

$${\sigma_{bi}}^2 = {R_\lambda}^2 \Sigma_{j=1}^{W} P_s(b_i) P_{xj} + 2q\left[R_\lambda P_s(b_i) + R_\lambda \Sigma_{j=1}^{W} P_{xj}\right]B_e + (4kTB_e)/R \quad for\ b_i \epsilon \{0,1\} \tag{15}$$

4.2 Worst case reliability analysis of PNoCs

A typical die size of 20mm X 20 mm is considered for the BER study. The maximum power launched is 1.5 mW, because a higher launched power than 1.5mW will cause resonance shift in the thermally tuned MRRs [16]. The signal losses for different topologies and their BER calculation are given in the following subsections. The worst case contributions of optical elements to the optical losses in the different topologies are summarized in table 4-2.

PNoC	N_{mrr}	N_{bend}	N_{λ}	N_l(cm)	SL(db)
Corona	124	16	0.79	20	42.2
Clos	126	2	0.78	5	13.6
2DFT	S*	11	2.08	7.725	35.7
MSB	130	4	0.8	3.65	10.5

*N_{mrr} – Number of MRRs, N_{bend}-Number of Bends, N_l- Length in cm. SL - Signal loss in db. *S – 2DFT uses switches which are explained in section 5.2.4*

Table 4-2 Photonic Elements along the path for Different PNoC Architectures

4.2.1 MSB PNoC

The MSB PNoC uses segmented photonic links to transfer data between nodes. The length traversed by a packet does not increase with the increase in size of the NoC. The data is sent across the network in a maximum of three hops and the data is regenerated for each hop. The worst case reliability is encountered in the single longest link in a MSB. The longest single link in a MSB is from cluster 1 to cluster 10 inside a super-cluster. The cluster 1 in RC(1) will communicate with cluster 10 in RC(3) through two segmented waveguides connected by an ISR and the total length travelled by the photonic packet is 3.65 cm. In the MSB PNoC, each photonic

waveguide contains 60 wavelengths and the packet will encounter 130 MRR pass-through losses. With 60 wavelengths per waveguide, the space between two adjacent wavelengths (Δλ) is 0.8nm. The crosstalk loss is -21,-27, and -30 db for the first, second, and third adjacent wavelengths [14].

4.2.2 Corona PNoC

Corona is an all photonic PNoC, which provides one to one connection to all clusters present in the architecture. A waveguide originating from a given cluster traverses through all the clusters in the PNoC architecture and terminates at the originating cluster. There are N waveguides in N-cluster corona architecture. In a 64-cluster corona PNoC, there are 8 rows with 8 clusters each. The photonic packet from cluster 2 in row 1 will traverse through all the eight rows and reach cluster 1 in row 1 in a 20 cm link, making it the longest. Each link in a corona has 63 Modulator MRRs and 63 Demodulator MRRs. Hence in worst case condition, a packet has to traverse through 124 intermediate MRRs, leading to 124 times the MRR pass through loss. Also, the link has 16 bends along the path. With 63 wavelengths, the spacing between two adjacent wavelengths (Δλ) is 0.79nm. The crosstalk between the first, second and third nearest wavelength is -21,-27, and -30 db respectively.

4.2.3 Clos PNoC

The Clos PNoC is a hybrid architecture, which uses both electronic and photonic links to send data. It uses 8x8 electronic cross-bars along with photonic links to transfer data between clusters. Clos PNoC consists of 8 clusters grouped into one

tile. Every tile has its own router to communicate with the other tiles. The eight clusters in a tile are connected to each other through electronic links. The communication between tiles takes place through hybrid links consisting of both photonic and electronic links. The inter tile communication takes place through two hops. The signal loss in photonic link is only considered because the electronic links are short and the degradation in electronic link is negligible when compared to the long photonic links. The longest photonic link is between two routers in tile 1 and tile 2. The longest distance travelled will be 5 cm in the U-shaped layout of waveguides in Clos PNoC

Each photonic link supports 64 different wavelengths. Hence there are 64 MRR modulators and 64 MRR demodulators. A packet on the photonic link has to pass through 126 MRRs. With 64 wavelengths on a waveguide, the space between two adjacent wavelengths ($\Delta\lambda$) is 0.78nm. This leads to a crosstalk loss of -21,-27, and -30 db for the first, second, and third adjacent wavelengths.

4.2.4 2DFT PNoC

The 2DFT is a hybrid architecture which uses electronic links to setup path for the photonic packets. The photonic paths to be used by payload flits are laid out by electronic control headers by turning on or off photonic switching elements. The packets are injected from the GS. GS contains the modulator and demodulator MRRs. The IS injects the packet generated by the GS into the network. The NS turn the photonic packet towards the destination. The final switch before the packet reaches the destination cluster is the ES. The packet makes its final turn on this switch to

reach the GS. The Header flit which is an electronic packet has the intermediate addresses for the IS, NS, and ES, the packet should be affected. The Electronic router sets up the path for the following photonic packet. The electronic header flit flows through the electronic path and sets up the MRRs for photonic switching. The photonic to electronic conversion of the packet will only take place in the destination cluster. The photonic packet simply flows through the path laid by the electronic header flit. The packet being degraded in an electronic path setup packet is negligible when compared to the photonic links. The packets are short in the path setup network and it uses guaranteed-delivery protocols [10] to ensure the reliability. The longest distance travelled by a packet on the photonic path in a 2DFT is 7.725 cm in the worst case condition, as the packet travels close to the total periphery of the die. The packet has to pass through 6 insertion switches, 7 Ejection switches and 14 network switches. The losses associated with these switches are given in table 4-3.

Source	Loss
Waveguide crossing loss	0.05dB
IS Pass-Through loss	0.36dB
Loss at IS	0.55dB
IS Pass-Through loss	0.25dB
Loss at IS	0.55dB
loss at an NS	0.71dB

Table 4-3 Losses from Various Switches in 2DFT [10]

The BER of different PNoCs, as a function of launched power is shown in fig. 4-1 for all the PNoCs discussed in this paper. The BER of the PNoCs decreases as the power launched per bit increases. The MSB PNoC considered for the reliability analysis contains two wavelengths per link to increase the link bandwidth rather than single wavelengths. This increases the number of MRRs on the photonic link of MSB PNoC making it similar to that of the other PNoCs as seen in table 4-2. Hence, the amount of MRR pass-through losses, cross-talk loss in a MSB PNoC is almost same as in all the other PNoCs considered for the study. Therefore, the distance travelled by the photonic packet on the optical fiber plays an important role in determining the difference in reliability of the PNoCs.

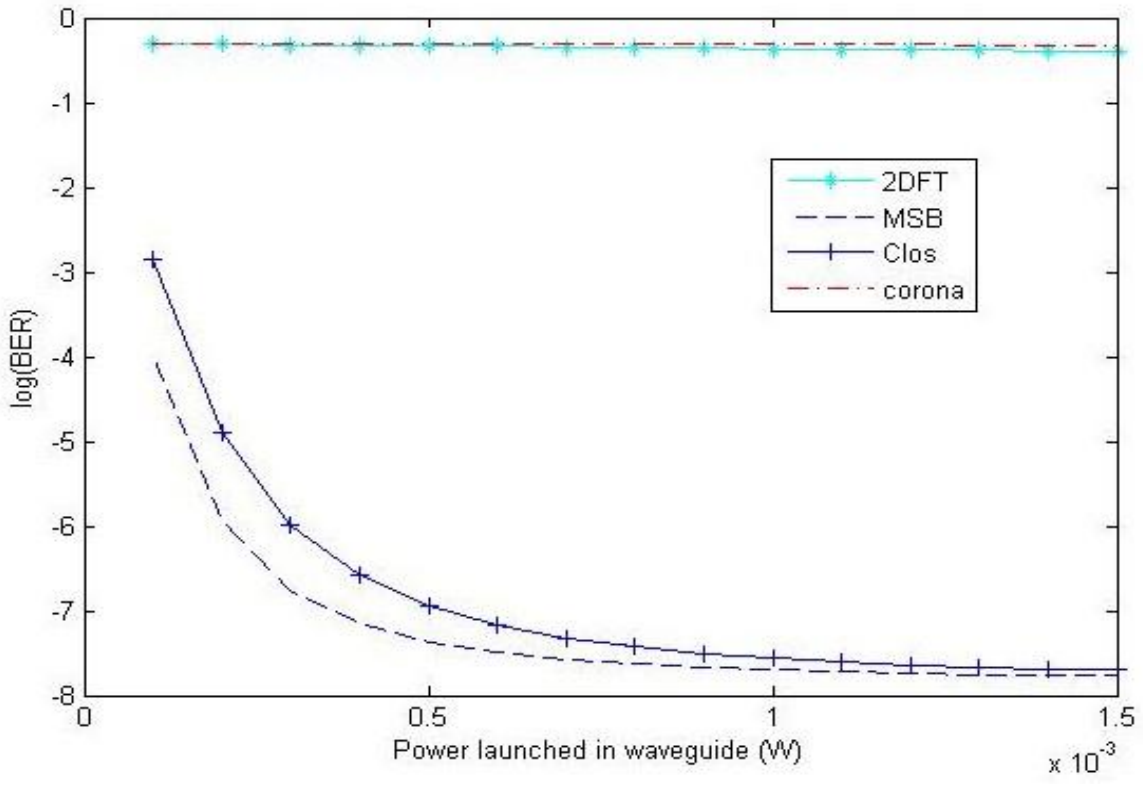

Figure 4-1 BER Characteristics of 64 Cluster PNoCs

The MSB has the least BER and hence is the most reliable PNoC architecture. The BER of the NMSB architecture is the same as the MSB as the worst case signal loss remains the same in both of them. The reliability of the Clos is similar but slightly higher than that of the MSB. The BER of the Corona and 2DFT are significantly higher than the Clos or the MSB. The BER of the MSB PNoC is better than Clos PNoC, because length travelled by a photonic packet in MSB PNoC is lesser than that of a Clos PNoC. The reliability of the corona PNoC is drastically affected due to the long serpentine path travelled by the photonic packet. The signal loss from the injection and ejection switches used in the 2DFT PNoC negatively affects its reliability. Also, the length travelled by a photonic packet in the worst case in a 2DFT is higher than MSB PNoC and Clos PNoC.

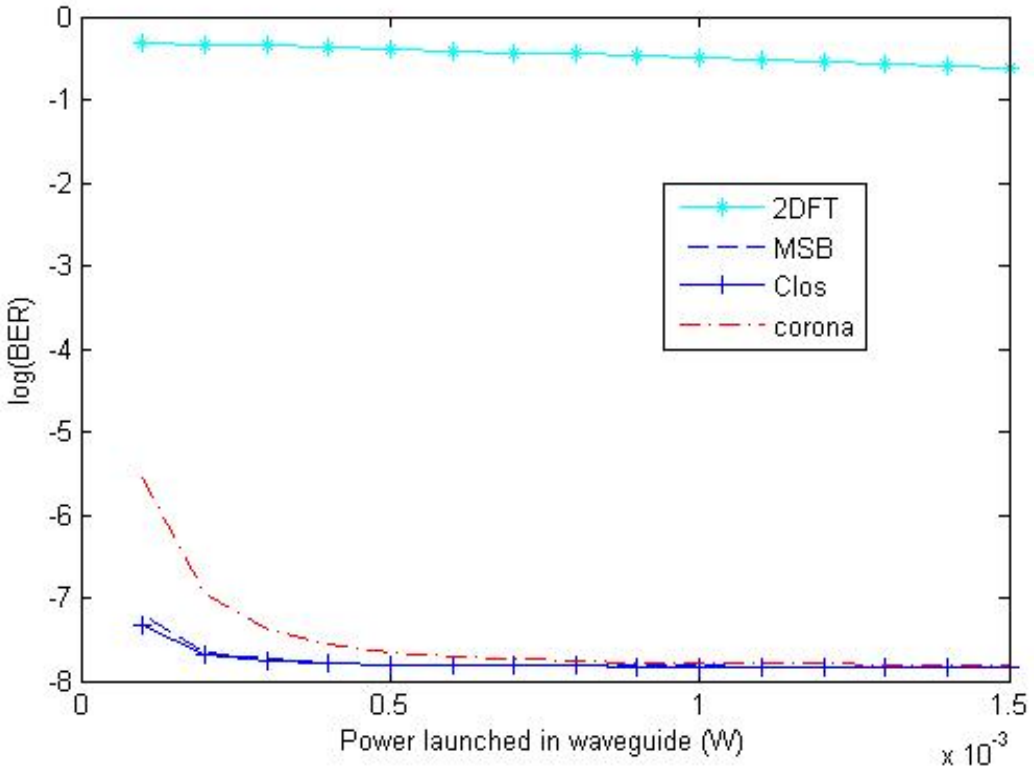

Figure 4-2 BER Characteristics of 64 Cluster PNoCs with new optical fiber.

With the advancements in the fabrication of optical elements such as MRRs and optical fibers, reliability of the PNoCs can be increased. In [17] a new optical fiber is demonstrated with path loss confined to 0.3db/cm and bending loss to 0.0002db/90^{o} bends. The distance, which the photonic packet travels, is a principal component that affects the reliability of the corona PNoC due to its long serpentine paths. With better optical fibers, the waveguide loss decreases. Hence, the BER characteristic of the corona improves significantly and closely matches with the MSB and Clos PNoCs. The BER characteristics of the 64 cluster PNoCs with the new optical fiber developed in [17] is shown in fig. 4-2.

4.3 Performance – Reliability trade off

The BER for the NMSB-PNoC is lower than the BER of other PNoCs for the same launched power. Various performance metrics shows the achievable trade-offs for

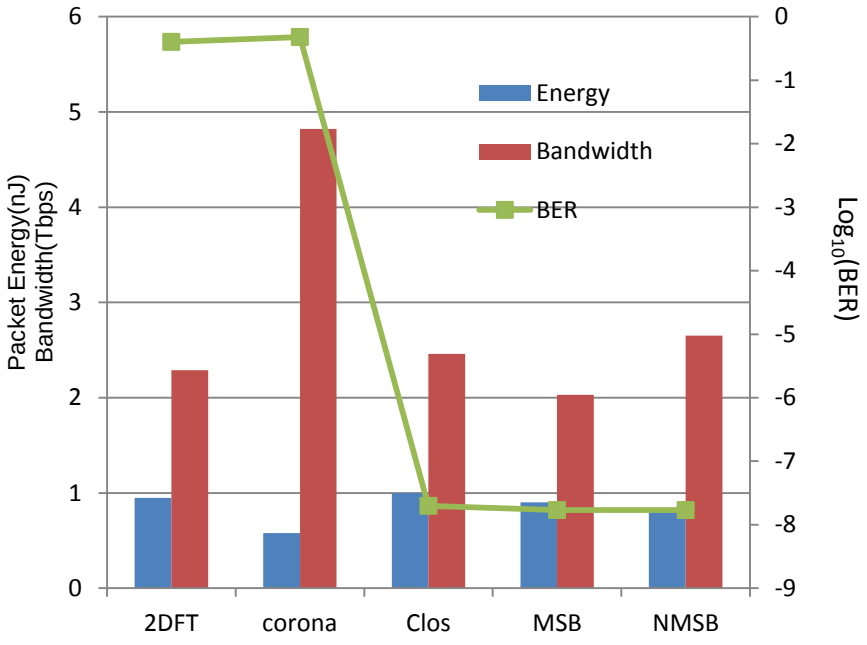

Figure 4-3 Packet Energy and BER of different PNoCs

the NMSB among the other PNoCs. The increase in reliability is due to the transfer of packets in multiple hops across the photonic network in NMSB PNoC. This prevents the photonic packets from travelling long distances on optical fiber, before regeneration. For each hop, packet should go through optical-electrical-optical conversion. However, this increases the latency and decreases the achievable bandwidth of the network. The performance is increased at the expense of reliability in corona PNoC, which has a single hop dedicated channel between every cluster.

In 2DFT, the special switches and higher PM improves the performance at the expense of reliability. The Clos, MSB and NMSB have lower bandwidth but also significantly lower BER compared to the Corona and 2DFT architectures. Fig. 4-3 shows the packet energy, peak bandwidth and BER for different PNoCs. Despite the multi-hop links, NMSB PNoC has lesser packet energy, because the packets spend less time waiting on the buffers. The corona and 2DFT PNoCs have higher packet energy, because of the energy spent on storing packets in the electronic buffers. Thus, the NMSB has better reliability than other PNoCs with better packet energy.

Chapter 5 Experimental Results

In this section we evaluate and compare the performance of various PNoC architectures discussed in this paper. Peak sustainable bandwidth, packet energy dissipation, and latency of packets are considered as the performance metrics in this paper. Peak sustainable bandwidth is defined as the maximum rate at which the NoC is able to route data successfully at saturation. Packet energy is the average energy dissipated in successfully delivering an entire data packet from source to destination when the network is saturated. Average latency is the number of cycle taken by a packet on an average to reach the destination, after it is injected into the network. Different application based non-uniform traffic scenarios are used to evaluate the different PNoC architectures studied here.

We use a cycle accurate NoC simulator to monitor the progression of flits per cycle accounting for all flits that reach the destination as well as those dropped. Photonic switches, made of MRRs convert the electrical packet into photonic packet and vice versa within one clock cycle [13]. In our experiments each cluster is considered to consist of a single core associated with a switch. Each port of a switch consists of 8 virtual channels with buffer depth of 64 flits. Each packet is divided into 64 flits and each flit is 32 bits wide. The link bandwidth is considered to be 10 Gbps per wavelength. The electronic components of the PNoCs are designed in RTL and synthesized using 65nm standard cell libraries from CMP [18]. A clock frequency of 2.5GHz is considered to be driving the switches and buffers. A hundred thousand iterations were performed for each simulation to reach stable results eliminating

the transients for the initial few thousand cycles. In the following subsections we present each of the experimental results.

5.1 Packet Energy Dissipation

There are several components of packet energy dissipation as data is transferred over the PNoC fabrics. The energy dissipated in a PNoC is given by equation (16),

$$E_{packet} = E_{electrical} + E_{photonic} \quad (16)$$

Energy dissipated by the photonic components is given by equation (17),

$$E_{photonic} = E_{launch} + E_{modulation} + E_{tuning} \quad (17)$$

Where, E_{launch}, $E_{modulation}$, $E_{tuning,}$ and E_{buffer} are the energy dissipated at launching photonic signals from light source, modulation/demodulation, tuning of MRR, and storing in buffer respectively. The energy dissipation per bit for various components of a PNoC is given in table 5-1.

Component	**Energy in pJ/bit**
$E_{Modulation}$	0.04/bit
E_{Tuning}	0.24/bit
$E_{Buffers}$	0.078125/bit
$E_{Launched}$	0.15/bit
E_{Router}	0.625/bit

Table 5-1 Energy of different photonic components [7]

A Launched power of 1.5mW is considered for the performance simulation, as it is the maximum power that can be launched without affecting the resonance of MRRs [14]. The MRRs consume energy for modulation/demodulation and for tuning to specific frequencies. Fig. 5-1 shows that the packet energy dissipation of an

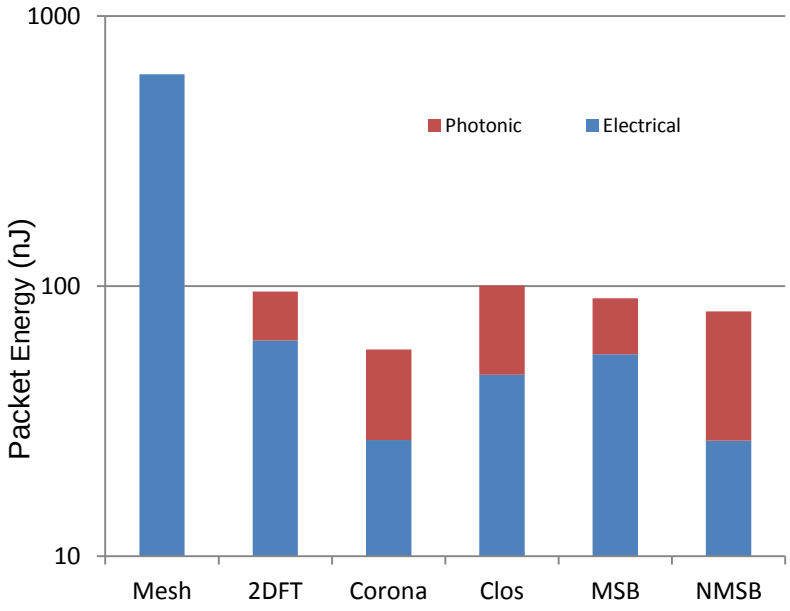

Figure 5-1 Packet energy of different PNoCs

electronic mesh NoC (Emesh) and the PNoCs considered in this work such as, 2DFT, Corona, Clos, MSB and NMSB architectures at network saturation for 64 core systems. Uniform random traffic is considered for the experiment. It can be observed that the packet energy dissipation of Corona is the least among all the PNoCs. This is because Corona has dedicated single-hop links between each source/destination pair. In 2DFT the packet energy is higher than Corona as the electrical path setup by the header flits results in higher electronic energy dissipation. Also more MRRs dissipate the tuning energy in the 2DFT. The Clos PNoC

has multi-hop network with electronic routers in the path of a packet. This causes the packet energy of the Clos to be the highest. The MSB PNoC has a blocking, multi-hop architecture. In a MSB PNoC, inter cluster communication will be blocked by intra cluster communication. The O-E-O conversion at every hop and higher latency leads to high packet energies in Clos and MSB PNoCs. The NMSB has lesser packet energy dissipation, because the dedicated non-blocking links in NMSB are faster than the MSB, with two channels per source and destination pair, inside super clusters. The non-blocking nature of the NMSB reduces the waiting time of a packet in a buffer consequently reducing the electronic component of packet energy significantly. The photonic component in the NMSB increases due to more photonic links required creating the non-blocking architecture; however, overall the NMSB reduces packet energy compared to MSB, Clos as well as 2DFT. However, all the PNoC architectures are considerably energy-efficient compared to the completely electronic mesh NoC due to the ultra-low power photonic interconnects.

5.2 Bandwidth

The amount of data that can be sent across a PNoC is determined by the availability of links and the speed of those links. Fig. 5-2 shows the peak achievable bandwidth for the PNoC architectures considered in this paper and an electronic mesh based NoC (Emesh) with uniform random traffic for 64 core systems. The flits are injected into the NoC at a rate of 1 flit per core per cycle by the cores.

All the PNoC architectures studied here have higher bandwidth compared to the electronic mesh due to the high bandwidth photonic interconnects. In 2DFT, each

source and destination pair consists of multiple channels between them. The photonic packet will be transmitted to the destination in a single hop. In order to have a non-blocking architecture in 2DFT, the PM should be equal to the number of clusters in PNOC. In corona, there is a single channel between every other source and destination. Due to the maximal use of DWDM in the waveguides of corona, the bandwidth cannot be increased further, just by increasing the number of channels available in the waveguides. The reliability of the corona PNoC will be affected when the number of wavelengths is doubled to increase the bandwidth, due to crosstalk. The Clos uses three routers for every inter-tile communication. The multi-hop data transfer, with a single wavelength between source and destination, affects the bandwidth. Also, the speed of the electronic routers determines the rate of data transfer. In a MSB PNoC, the inability to perform inter-cluster and intra-cluster communication at the same instance affects the bandwidth. The packets are

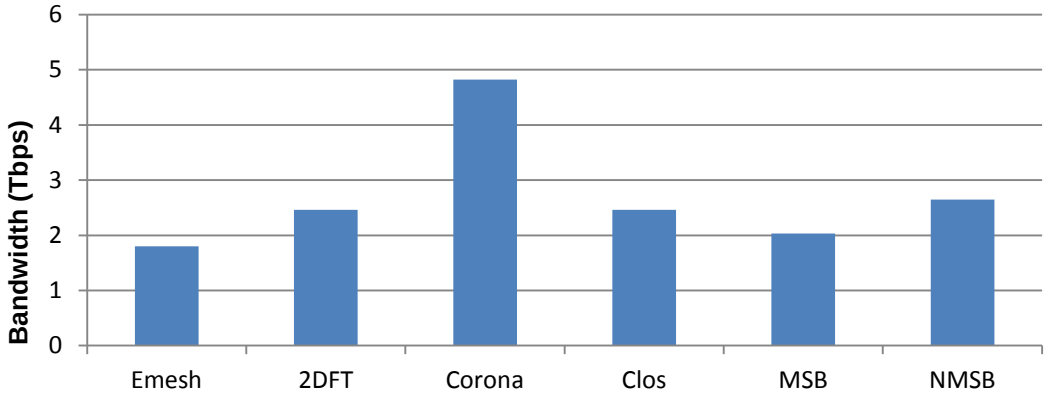

Figure 5-2 Peak bandwidth of different PNoCs

buffered due to occupied links in MSB-PNoC. On the other hand, the NMSB strikes a balance between reliability and available bandwidth.

The proposed NMSB has a non-blocking architecture with multiple hop connections between all source and destination pairs. Also, there is no routing logic between the hops. This reduces the path loss and enables highly reliable data transfer in each hop in the NMSB architecture without significantly compromising performance. The NMSB has two channels for sources and destinations, within the same supercluster and separate channels for inter super cluster communication creating the non-blocking architecture. Consequently, the NMSB has better bandwidth than Clos and MSB. Due to a single hop connection between source and destination, corona PNoC has highest bandwidth among all the PNoCs.

5.3 Performance evaluation with application-specific traffic

In this section we evaluate the performance PNoCs with application specific traffic patterns from parallel benchmark suites like SPLASH-2 [19] and PARSEC [20]. Application-specific traffics are obtained using GEM5 [21], a full system simulator, to obtain detailed processor and network-level information. We consider a system of 64 alpha cores running Linux within the GEM5 platform for all experiments. The memory system is MOESI_CMP_directory, setup with private 64KB L1 instruction and data caches and a shared 64MB (1MB distributed per core) L2 cache. We consider three SPLASH-2 benchmarks, FFT, RADIX, LU [19], and the PARSEC benchmark CANNEAL [20] that vary in characteristics from computation intensive to communication intensive in nature and thus are of particular interest in this work. The behavior and problem size of the benchmarks is described in Table 5-2.

Benchmark	Busy %	Idle %	Default Problem Size
FFT	81.99	18.01	65,536 Data Points
RADIX	84.98	15.02	262,144 Integers, 1024 RADIX
LU	87.62	12.38	512x512 Matrix, 16x16 Blocks
CANNEAL	56.74	43.26	200,000 Elements

Table 5-2 Behavior and problem size of the benchmarks [19][20]

The same traffic pattern is used for all the PNoCs for uniformity of comparison. The original frequency of traffic interaction between the cores is obtained from GEM5 and used to generate the traffic patterns for each benchmark in a cycle-accurate NoC simulator to obtain the NoC performance in terms of packet energy. The packet energy of PNoCs for different benchmarks is shown in fig. 5-3.

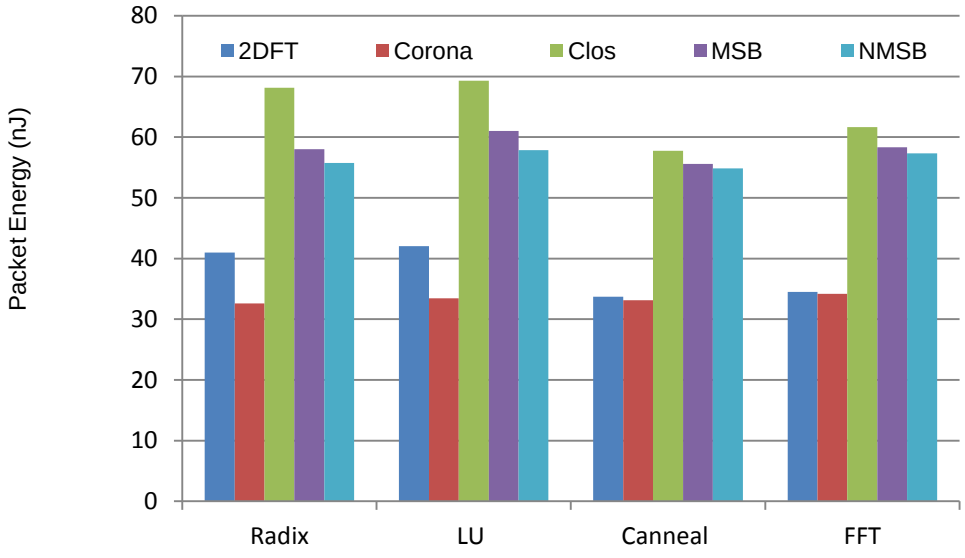

Figure 5-3 Packet energy of different PNoCs under various application specific traffic patterns

The benchmarks, which emulate the application based traffic patterns, may produce skewed traffic on some parts of the network. The flits will be stalled in buffers if the link is occupied and the packets may be dropped due to unavailable

links and storage buffers. In such cases, the PNoCs, which have the single hop dedicated links between source-destination pair, will dissipate lesser packet energy. Hence, the multi-cycle, multi-hop hybrid links of the Clos PNoC along with its electronic routers on the path results in highest packet energy among the PNoCs considered in this paper. On the other hand the Corona PNoC with its single hop dedicated links between source and destination has the least energy among the PNoCs for all traffic patterns used in the experiment.

The 2DFT with full path multiplicity, which also has dedicated single hop photonic links between all nodes, has higher energy than the corona PNoC because of its underlying blocking electronic mesh architecture, which is used by the header flit for setting up the path. Despite the multi-cycle and multi-hop links in both MSB and NMSB PNoC, the NMSB has lower packet energy than MSB PNoC due to its non-blocking links. The NMSB has multiple links between the source and destination, due to the use of special segmented buses. This helps in alleviating the problem of skewed traffic distributions and hence the NMSB architecture is able to achieve the lower average packet energy than the Clos and MSB PNoC in all the application based traffic scenarios studied here.

5.3 Performance evaluation with higher system sizes.

Due to the use of segmented bus architecture NMSB PNoC, it can be scaled up to systems with larger number of clusters. Length of the photonic link, number of MRRs, and number of wavelengths of the SB_{mn} and SB_{nm} in the super clusters, are not increased by increase in system size. The non-blocking architecture can be

achieved by increasing the path multiplicity in IGBs, SB_{mg}s, and SB_{gm}s. Hence, reliability of the NMSB PNoC is not affected by the system size. Fig. 5-4 shows the packet energy of 64 and 128 cluster NMSB PNoCs along with the worst-case BER.

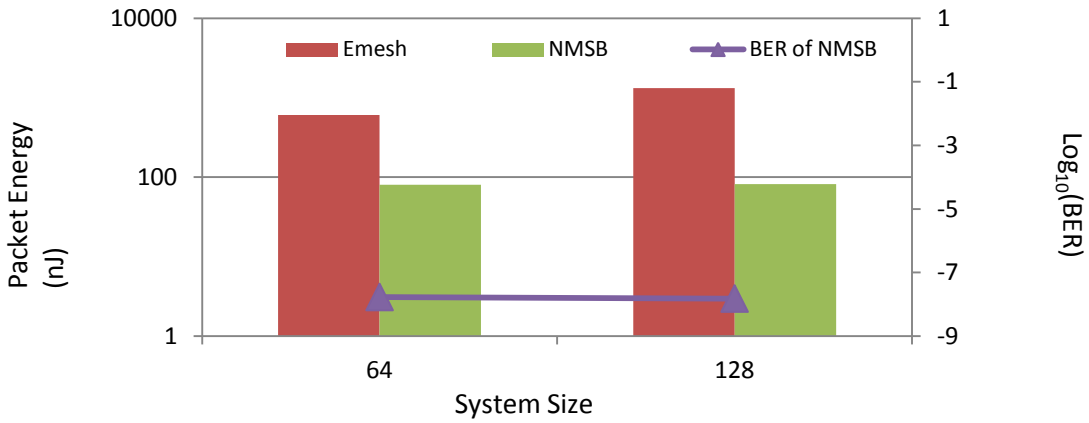

Figure 5-4 Packet energy and BER of NMSB PNoC for different system sizes.

The packet energy of the 128 cluster NMSB is not significantly higher than that of the 64 cluster NMSB as the maximum hop-count between clusters remain the same. The maximum hop-count does not increase in the case of the 128 cluster NMSB as the inter-supercluster communication occurs through the same IGBs making this architecture extremely scalable. Table 5-3 shows the maximum and average hop-counts of the NMSB architectures of various sizes considered here. The average hop-count in the NMSB increases much less compared to the increase in case of an electronic mesh. Hence, the increase in packet energy is significantly higher in a mesh based NoC than in an NMSB PNoC. On the other hand, the BER actually decreases as the size increases due to reduction in length of the local segmented busses in the NMSB architecture.

System Size	Mesh		MSB-PNoC	
	Avg.	*Max*	*Avg.*	*Max*
64	5.33	14	2.12	3
128	8	22	2.32	3

Table 5-3 Average and Maximum Path Length in No. of Hops

5.4 Area Overhead

The optical elements such as MRRs and optical fibers required for building the PNoC can be fabricated on a separate layer in the chip [22]. Fig. 5-5 shows the area overheads of the photonic devices and length of photonic waveguides required for realizing the various PNoC architectures considered in this work.

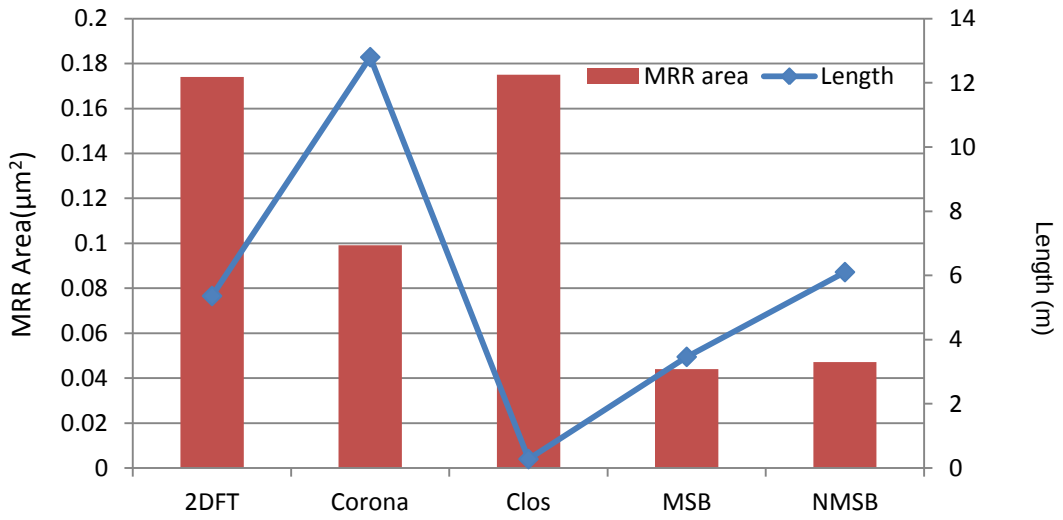

Figure 5-5 Area overhead of different PNoCs

In our study, we have considered MRRs of size 4um in diameter [7]. Also, the MRRs can be fabricated in vertical fashion in places where path multiplicity is used [23]. With the help of segmented waveguides, length of the photonic waveguides that has to be laid on the PNoC is reduced in NMSB and MSB PNoCs. The segmented

waveguides are shared by many clusters in a row. In corona PNoC, a long waveguide is associated with every cluster. The waveguides are shared efficiently in the Clos PNoC with the help of electronic routers, facilitating the less use of optical fibers. But when the optical fibers are shared between clusters, they must be able to support more wavelengths for better performance. We can see from the figure that the Clos PNoC has the highest area occupied by MRRs due to large number of wavelengths and MRRs associated with them. The NMSB PNoC strikes a balance between both the extremes primarily due to the shared segmented bus based architecture.

Chapter 6 Conclusion

In this paper we have presented the performance evaluation of a reliability aware NMSB PNoC architecture. The NMSB PNoC provides competitive performance and energy-efficiency with respect to the other PNoCs. Estimates of area overheads and length of waveguides used the MSB based architectures have significantly less overheads compared to the other PNoCs. In summary, the NMSB architecture achieves the lowest average packet energy dissipation while, the highest bandwidth is achievable in the Corona architecture. The BER of the 2DFT architecture is among the highest while the BER of the NMSB and MSB architecture is the lowest signifying that those are the most reliable PNoC architectures.

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